X Series USRP-LW X310

The USRP-LW X310 is a high-performance, scalable software-defined radio (SDR) platform for designing and deploying next-generation wireless communication systems.

The USRP-LW X310 hardware architecture combines two expanded bandwidth daughter board slots with a bandwidth of up to 160M from DC to 6GHz. And it features multiple high-speed interfaces to choose from (PCIe, Gigabit/10 Gigabit Ethernet ports), as well as a resource-rich, user-programmable Kintex-7 FPGA. In addition, the USRP-LW X310 uses an open source cross-platform UHD driver, with a large number of development frameworks, compatible reference architectures, and open source projects.

As the digital processing core of the USRP-LW X310, the XC7K410T FPGA provides high-speed connectivity between all major components. Includes RF front end, host interface, and DDR3 memory. The default FPGA provides all UHDs for controlling digital downconversion and digital upconversion, fine frequency tuning, and some other DSP function blocks. Users can take advantage of the spare space of the resource-rich Kintex-7 FPGA, plus the RFNoC development framework supported by USRP, to develop and implement their own DSP processing modules.

The USRP-LW X310 Equipment Kit includes: one **USRP-LW X310 main unit, Gigabit cable, SFP+ Gigabit adapter, power adapter, USB2.0 JTAG cable, SMA connector RF cable 4 root.**

Performance comparison table of FPGA of the Ethernet Port Series and X Series

	USRP-LW N210	USRP-LW X310
FPGA	Spartan3XC3SD3400A	Kintex 7 -410T
Logic Cells	53k	406k
Memory	2,268 Kb	28,620 Kb
Multilliers	126	1540
Clock Rate	100 MHz	200 MHz
SyreamingBandwith per Channel(16-bit)	25 MS/s	200 MS/s

The USRP-LW X310 offers a variety of high-speed interfaces to choose from. On the panel of the device, the Gigabit Ethernet port is one of the simplest and most commonly used ways to connect. For applications with extended bandwidth and low latency, such as PHY/MAC studies, the X310 provides an efficient bus interface PCIe x4 for this deterministic operation. When the application uses network recording or multi-node processing, 10 Gigabit port is the best choice.

The USRP-LW X310 includes many additional features that will help some other wireless applications. For example, in FPGA design, the 1GB DDR3 on the motherboard can be used as data buffering and data storage. The optional internal GPSDO provides high-precision frequency reference when synchronized to the GPS system with a synchronization delay of less than 50ns. Allows the user to control external components such as amplifiers and switches through the GPIO interface, support inputs such as event triggers, and observe debug signals. The USRP-LW X310 also includes an internal JTAG adapter that allows developers to easily load and debug new FPGA images.

USRP-LW X310 technical data:

Parameter category	numeric value	unit	Parameter category	numeric value	unit
Input/Output			**RF performance parameters when paired** with **SBX-LW 120**		
DC voltage input	12	V	Single-sideband signal/image rejection	-35/50	dBc
Power consumption	45	W	**Phase noise**		
Convert module parameters			3.5GHz	1.0	degRMS
ADC sampling rate (max	200	MS/s	1MHz	1.5	degRMS
ADC resolution	14	bits	Output power	> 10	dBm
DAC sampling rate	800	MS/s	Enter a third-order intercept point	0	dB
DAC resolution	16	bits	Noise figure	8	dB
With host maximum rate (16b).	200	MS/s	**Physical properties**		
Local vibration accuracy	2.5	ppm	Operating temperature	0-55	C
GPSDO precision is not locked	20	ppb	size	290×225×50	mm
			Weight (2 sheets SBX-LW 120).	1.8	kg

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